Muhammad Shuaib

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Nationality: Pakistani
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Academic Qualification:

MSc Electrical Engineering (System on Chip), **2 Years**

Linköping University Sweden, (2009**) GPA (3.44/4.0)** (Converted from ECTS and Swedish grade systems)

BSc Electrical Engineering (Major in Electronics and Communication); 4 Years. 1st Division.

University of Engineering and Technology Taxila Pakistan.

BSc (Applied &Pure Mathematics, Physics); Two Years,

University of the Punjab Lahore, Pakistan. **1st Division.**

Research Projects:

(a) Mm wave-LNA Project:(During 2022 and on word)

This project is aimed at mm-wave receiver, which is an important part of mm-wave transceivers. In future high data rate wireless communication systems, high resolution radars etc would be an integral part of 5G systems and other related applications. I am working on this project to design chip for this receiver in CMOS technology. LNA (Low-noise amplifier) being the crucial part of this design, where a weak signal is amplified along with noise. I have designed D-band LNA at an operating frequency of 60GHz, its results have been published in 4th ACM International Conference on Electronics Communication (**July 8-10, 2022), Tokyo, Japan.**

Publications:

1: Muhammad Shuaib, "60 GHz,12mW,20 dB Gain, CMOS mm-Wave LNA with 6.3-dB NF" 4th ACM International Conference on electronics communication (**July 8-10, 2022), Tokyo, Japan** (**EI Compendex, Scopus etc**).

Apart from it second most important block of this receiver ismMixer, I am working on this block to realize a complete receiver and finally a complete chip for mm-wave receiver and of course more publications regarding this project

(b) Δ-Σ ADC for High Speed Wireless Devices (During 2022 and on ward)

Δ-ΣADC being an important part of future mixed-signal wireless devices. I am also working on this research project to design in 45 nm CMOS Process. In this regard I have designed a three stage OTA (Operational Transconductance amplifier) in a 45 nm process.

Publications:

1: Muhammad Shuaib "Low-voltage, high-speed three-stage class AB CMOSTA hybrid of RNIC and NMC techniques" manuscript submitted (under review) in leading IC design journal

This project is in continuous phase. I want to design a complete chip for this Δ-ΣADC and hopefully I will publish more journal publications regarding this project.

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Publications

Journals:

1: Low-voltage, high-speed three-stage class AB CMOSTA hybrid of RNIC and NMC techniques" manuscript submitted (under review) in leading IC design journal.

Peer Review Conferences

2**: Muhammad Shuaib**, "60 GHz,12mW,20 dB Gain, CMOS mm-Wave LNA with 6.3-dB NF" 4th ACM International Conference on electronics communication (**July 8-10, 2022), Tokyo, Japan** (**EI Compendex, Scopus etc**)
https://dl.acm.org/doi/fullHtml/10.1145/3560089.3560091

3: **Muhammad Shuaib**, "110dBΩ,336MHz Band width, Low Noise Trans-Impedance Amplifier". IEEE the 4th International Conference on Circuits, Systems and Simulation, **May 26-28, 2021, Malaysia**. (**EI Compendex, Scopus, etc**)

4**: Muhammad Shuaib**, "92dB DC-Gain Two-Stage Class AB Fully-Differential Op-Amp" IEEE the 5th International Conference on Integrated Circuits and Microsystems, **October 23-25,2020, China**. (**EI Compendex, Scopus, etc**)

MSc Thesis:

5: **Muhammad Shuaib**, "Two-Tone PLL For On-Chip Test In 90nm Technology" **(2009)** ISRN: LiTH-ISY--EX--09/4311—SE OAI: oai: DiVA.org: liu-18590 DiVA, id: diva2:220552
http://liu.diva-portal.org/smash/record.jsf?pid=diva2%3A220552&dswid=-3090
@ Amazon.com
https://www.amazon.com/Two-Tone-PLL-Chip-RF-Test/dp/3639180895

Chip Design Projects:

1: ***CENIIT project 03.03*** **"*Testability-oriented Design Techniques for Mixed-Signal/ RF Integrated Circuits"***

In this project, principal investigator was Professor Jerzy Dabrowski at Linkoping university Sweden. Main goal was to develop testability-oriented design techniques for mixed signal/RF integrated circuits. My contribution in this project was to design a circuit regarding on-chip test for linearity. To achieve this objective, I designed "Two-Tone PLL For On-Chip Test In 90nm Technology" at system level, at the circuit and transistor level. This project was my MSc thesis. In later years, this PLL was fabricated and results were published in IEEE transactions. For more detail please follow this link.
http://users.isy.liu.se/en/eks/jdab/Ceniit03-03.html

2. "D***esign, Analysis and testing of DLL chip"***

In this project I learned how to design, tape out and test a chip. This project was taken in a complete semester course "VLSI Design (CDIO)". Through this project, I got an experience of all phases of chip, viz; system level design, circuit level, transistor level design, lay out and finally testing of chip after fabrication.

3. Apart from above, I have also done projects related to mixed signal processing system and digital IC domain at the system level, circuit level and transistor level.

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4: "***Design of high gain, good gain-bandwidth product, low power Op-amp for continuous time sigma-delta modulator"***

In this project, I designed two-stage op-amp with class AB as output stage for continuous-time sigma-delta modulator in 180nm TSMC CMOS process. Results of this project were published in "The 5th International Conference on Integrated Circuitsand Microsystems,**23, Oct,2020. China**.

5: " ***Design, analysis and simulation of TIA-Analog Front End (TIA-AFE) for optical sensing applications"***

I designed low noise, high gain transimpedance amplifier for optical sensing photo-receiver. This project has been designed by using CMOS AMI Semiconductor's C5 process. Results of this project were published in" The 4th International Conference onCircuits, Systems and Simulation **(May 26,2021**). **Malaysia**.

6: ***"LNA for mm-Wave Receiver (60GHz)***

I designed 60 GHz,12mW,20 dB Gain, CMOS mm-wave LNA with 6.3-dB NF for high data rate wireless communication systems by using EDA tool Cadence Virtuoso (IC614) and 130nm rf TSMC PDK. This research results are published in 4th ACM International Conference on electronics communication **(July 8-10, 2022), Tokyo, Japan.**

7. "***Low Voltage, High -Speed and High gain Three Stage OTA Design"***

I have designed low voltage, high-speed and high gain three stage OTA for high performance Pipeline ADC and Δ-Σ ADC", in 45 nm CMOS process. Its research results are submitted in leading IC design journal for publication.

8. "CT Δ-Σ Modulator for High -Speed Wireless Devices"

Presently I am working on this project, goal is to design CT Δ-Σ modulator for high -speed wireless devices with EDA tool Cadence Virtuoso (IC614) and 45nm process.

Experience:

1: Teaching Experience (01-01-2010 to date):

Presently I am Assistant Professor at International Islamic University Islamabad (Pakistan), in Electrical engineering department:

https://www.iiu.edu.pk/?page_id=2062

with responsibilities research and teaching. I teach Electronic Circuit Design Course, Analog Filter Design Course, VLSI Design Course, Micro Electronic Technology Course, Circuit Analysis (1&2 Courses). Basic Circuit Theory (BEE). Apart from this, I was also undergraduate in charge for one year. I am also member of the team who has established Advanced Electronic Lab. This project has been funded by IDB (Islamic Development Bank). During the execution of this project, I have worked with the Principal Investigator. I was part of

team who had conducted two national level workshops: National Workshop on ASIC Design and CMOS Processes (25 to 27-05-2011), in collaboration with National Centre for Physics (Quaid-e-Azam University, Islamabad).

https://www.iiu.edu.pk/?page_id=9715

and second workshop: National Workshop on Advanced Electronic: Device Design and Process Characterization (02-03.12.2013) funded by HEC (Higher Education Commission of Pakistan). In this workshop, HEC, Pakistan released amount in favor to

me for conducting this workshop. I have supervised various projects at undergraduate level. https://www.iiu.edu.pk/?page_id=14227

2: 2003- To- 2006 Assistant Manager (Electrical Engineer), GEPCO, Pakistan:

I have been working as Assistant Manager in (Gujranwala Electric Power Company) in Pakistan, which is one of the companies in Pakistan, which provides and distributes electricity to the consumers. I was member of the team whose responsibilities were to carry out testing and troubleshooting, especially the protection and instrumentation wing of the system.

3: 2002-To-2003Assistant Director, Punjab Industries (Electrical Engineer):

I have been working as Assistant Director in Punjab Industries, Mines and Mineral Department (Pakistan).

Grant:

Rs=559000/- by Higher Education Commission (HEC) of Pakistan to conduct workshop, National Workshop on Advanced Electronics: Device Design & Process characterizationon 02-03.12.2013. http://oric.iiu.edu.pk:4111/oweb/cws.php

Please read Sr No: 11, on above mentioned link

Reviewer and Session Chair Experience :

1: Reviewer of 11th International Conference on Communications, Circuits and Systems(ICCCAS 2022), held on 13-15-2022 at Singapore.
http://www.icccas.org/

2: I have chaired two sessions and also reviewer of 2020 IEEE 5th International conference on Integrated Circuits and Microsystems (ICICM2020) October 23-25China.
http://www.icicm.net/index.html

Interest Area:

Analog/Mixed-Signal IC design, RF/Analog circuits for wireless communication, Low-Power analog circuit design. Delta-Sigma Converters, Nyquist rate data – converters, Phase locked loops and CMOS Image Sensors. Optical receiver.

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EDA Tools Experience:

Cadence (HDL, Schematic, Virtuoso, LVS, Assura, Calibre, Spectre /Spectre RF), Mentor graphic IC Design. ADS. LT Spice, Hspice, Electric VLSI. High-Level circuit modelling languages such as VHDL, Verilog, and Verilog-A, MATLAB& Simulink.

Processes:

I have ability to work in micron, sub-micron, deep submicron, ultra-deep submicron CMOS processes

Social Skills:

I have ability to work independently as well as with in team. I have also experience to work with people of diverse social, cultural, and educational background this experience was obtained during my study in abroad (Sweden) and also through organizing, IEEE the 5th International Conference on Integrated Circuits and Microsystem Circuits and Microsystems, 23-25 October 2020, Nanjing, China**.**

Languages:

English: IELTS: 6 Band, Urdu: native, Punjabi: Fluent, French: Basic

References: On demand.